



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/826,179	04/04/2001	Keisuke Goto	KPM-01501	2868
26339	7590	05/05/2004	EXAMINER	
PATENT GROUP CHOATE, HALL & STEWART EXCHANGE PLACE, 53 STATE STREET BOSTON, MA 02109			LE, DINH THANH	
			ART UNIT	PAPER NUMBER
			2816	

DATE MAILED: 05/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application N .

09/826,179

Applicant(s)

GOTO ET AL.

Examiner

DINH T. LE

Art Unit

2816

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 2/5/04.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-9 and 17-24 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 24 is/are allowed.
- 6) ☒ Claim(s) 1-9 and 17-23 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

Art Unit: 2816

## NON-FINAL REJECTION

### Response to Applicant's Amendment

The rejections over Mnich (US6,346,839) is withdrawn in view of the Affidavit filed on 2/5/04.

### *Claims Rejections*

#### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-4, 6-7, 9, 17-19, 20 and 22-23 are rejected under 35 USC 102 (e) as being anticipated by Lee (US 6,229,368).

Mnich discloses in Figure 1 shows a DLL circuit comprising:

- a phase detector (111a) and a delay circuit having a variable delay section (111b) for generating an internal clock signal from a frequency variable clock signal (CLK); and
- a fixed delay section (111c, 112a) for generating a first internal clock signal (FCLK) at a second node (131); and
- wherein the delay time of the variable delay circuit (111b) is adjusted by the control signals (CNT) from a delay control circuit (111d).

Art Unit: 2816

With regard to claims 4, 6, 20 and 22-23 the fixed delay section comprising identical inverters (I1-I4) so that they have the same predetermined delay time independent from the input frequency since the delay time of the inverters are determined by the size of the transistors formed the inverters.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 5, 8 and 21 are rejected under 35 USC 103 (a) as being unpatentable over Lee (US 6,229,368).

Lee discloses in Figure 1 a DLL circuit comprising all of the limitations of the claimed invention as discussed above but does not disclose that each of the delay elements of the second delay section delays the first delay signal by an amount of time different from other delay elements as recited in claims 5 and 21, and each delay element comprises an inverter and a buffer as recited in claim 8. However, a skilled artisan recognizes that the delay time of each delay inverter of Lee can be selectable to offer a different time delay (phase shift) by selecting the size of the transistors of the inverter and employing a buffer after each inverter for isolating the inverters is well known in the art. Thus, selecting different delay time for each inverter of Lee and employing the buffers for isolating the inverters is a common practice and is considered to be a matter of a design expedient for an engineer depending upon a particular environment in

Art Unit: 2816

which the circuit of Lee is to be used. Lacking of showing any criticality, a skilled artisan would have been obvious to employ the buffer and select the delay time of the inverters of Lee for the purpose of isolating the inverters and accommodating with the requirement a predetermined system in which the circuit of Lee is to be used.

***Allowable Subject Matter***

Claim 24 is allowable because the logic circuit s (203) in Figure 9 of the applicant's admitted prior art does not generate an enable signal in synchronism with the first internal signal and a lath signal in synchronism with the first internal clock signal.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Dinh Le whose telephone number is (703) 305-3790. The examiner can normally be reached on Monday to Friday from 7:00 A.M. to 5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (703) 308-4876. The fax phone number for this Group is (703) 308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

April 26, 2004

DINH LE  
Primary Examiner

